TV Test Pattern Generator

Part 2

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This month we'll look at the colour encoder section and the power supply. A separate printed circuit board has been prepared for both of these and details, along with constructional and setting up details, will be given next month.

Coder and Modulator

The colour encoder takes in separate sync, red, green and blue signals (also the grey-scale signal) and produces a composite video output. This is available at v.f. or, via the modulator, at u.h.f.

The encoder/modulator circuit is shown in Fig. 6. The heart of the encoder is a Mullard i.c. (IC3), type TEA1002. A block diagram for this device is shown in Fig. 7. It has an internal 8·86MHz oscillator from which the R−Y and B−Y carriers are generated. Composite sync, burst gate enable, PAL switch and composite blanking timing signals are required in addition to the RGB and grey-scale inputs. The output is a 16-colour (including black and white) composite video signal, based on 75 per cent colour bars.

The RGB, composite sync and composite blanking signals are fed directly to the i.c. from the logic board where they are generated and inverted as required. The burst gate enable and PAL switch signals are generated on the colour encoder board from the composite sync signal. The grey-scale drive is also generated on the encoder board. The burst gate enable signal is derived from one half of IC4, type 4528, a dual retriggerable-resettable monostable. A CMOS device is used deliberately to introduce a small delay at the start of the signal. The *RC* network R4/C2 sets the pulse width at around 2·2μsec. The output goes to pin 15 of the TEA1002.

The other half of IC4 is used to provide a line frequency trigger pulse for one half of the 4013 dual D-type flip-flop IC5. This produces the 7·8kHz PAL switch signal which is fed to pin 12 of the TEA1002.

The three-bit binary-coded grey-scale information is fed to IC1 (a quad two-input OR gate) along with the grey-scale enable signal. The outputs from these OR gates (when enabled) are fed to sections of IC2 (hex driver with open-collector outputs) and arrive, via the three presets VR1, VR2 and VR3, at a common summing point that drives the TEA1002's luminance input (pin 7). FC2 is the most significant bit, causing a single transition from black to white. FC1 is the next most significant bit, producing the "almost black" and "almost white" bars. FC0 is the least significant bit, filling in the greys. The background enable signal simply inserts a level of grey, set by VR4, to lift the crosshatch background out of black.

Since the current capability of the video output from the

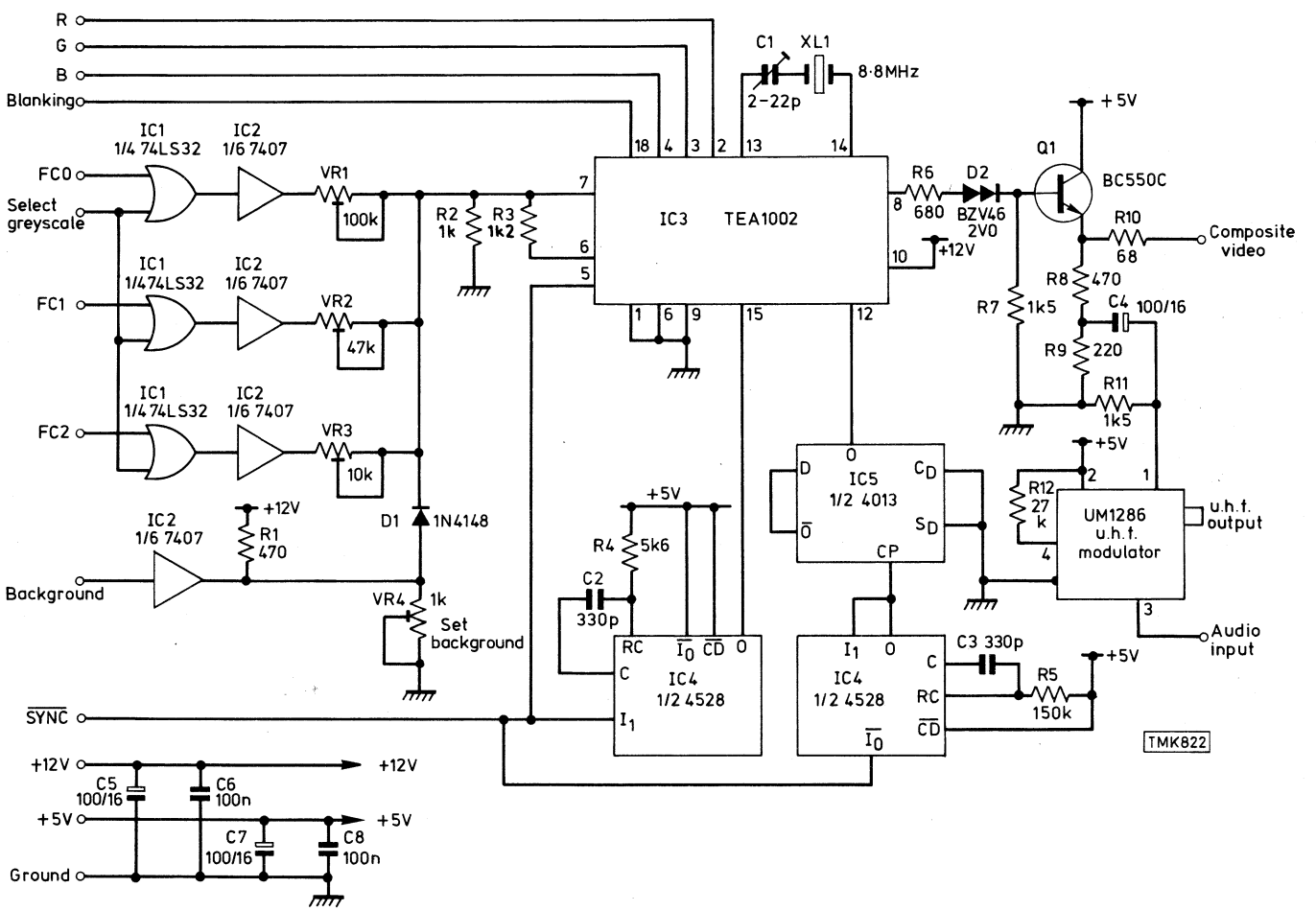

Fig. 6: Circuit diagram of the encoder and modulator sections of the pattern generator.

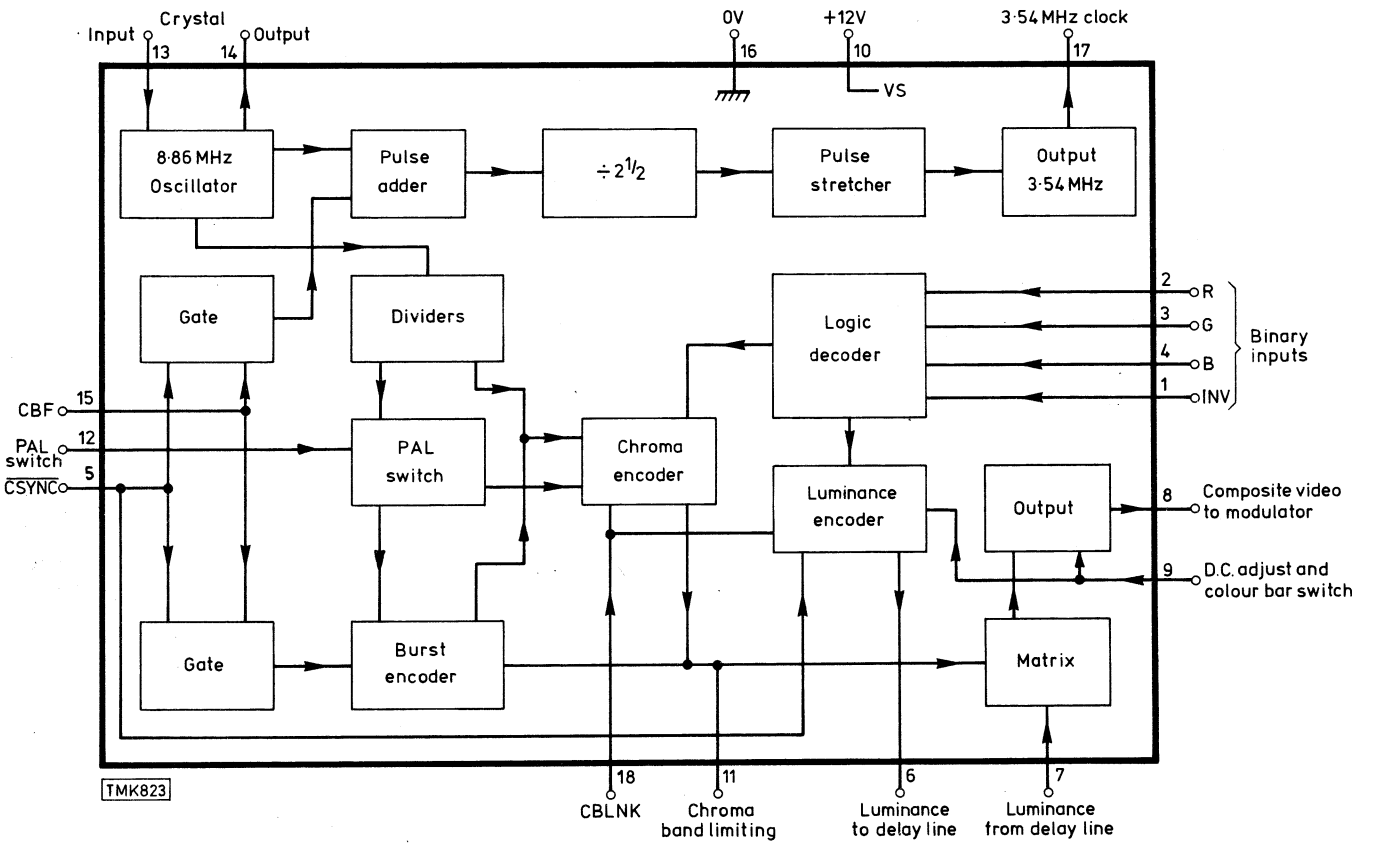

Fig. 7: Block diagram of the TEA1002 encoder i.c. The 3.54MHz clock output is not used.

Components list: encoder

Resistors:

R1	470
R2	1k
R3	1k2
R4	5k6
R5	150k
R6	680
R7	1k5
R8	470
R9	220
R10	68
R11	1k5
R12	27k

All ¼W, 5% carbon film

VR1	100k
VR2	47k
VR3	10k
VR4	1k

miniature skeleton presets, horizontal mounting

Capacitors:

C1	2-22pF trimmer
C2	330pF ceramic
C3	330pF ceramic
C4	100μF, 16V radial el.
C5	100μF, 16V radial el.
C6	0·1μF ceramic
C7	100μF, 16V radial el.
C8	0·1μF ceramic

Semiconductor devices:

D1	1N4148
D2	BZV46-2V0
Q1	BC550C
IC1	74LS32
IC2	7407
IC3	TEA1002
IC4	4528
IC5	4013

Miscellaneous:
XL1 8·8MHz crystal with HC18/U case
Astec UM1286 u.h.f. modulator. PCB.

Components list: power supply

C1	1,000μF, 25V axial el.	D1	1N4001
C2	1,000μF, 25V axial el.	D2	1N4001
C3	4,700μF, 16V axial el.	BR1	KLB02
C4	100μF, 16V axial el.	IC1	7812
C5	0·1μF ceramic	IC2	7802
C6	100μF, 16V axial el.		
C7	0·1μF ceramic		

Mains transformer RS 208-333, 18VA.
Heatsink 50mm length of RS 401-497 (for IC1/2).

TEA1002 is rather limited, a buffer transistor (Q1) is used. Resistors R6 and R7 reduce the input level at the base of this transistor to 2V peak-to-peak. The output is a 75Ω signal which is reduced to the normal 1V peak-to-peak when terminated at 75Ω. D2 is the equivalent of two diodes in series but giving a close-tolerance forward voltage drop of 2V. Its purpose is to remove 2V from the 2·6V d.c. pedestal on which the video signal sits. Q1's base-emitter voltage drop removes the residual 0·6V. In practice there's a very small residual d.c. voltage, though it's insignificant. D2 can be omitted if a 2V pedestal can be tolerated.

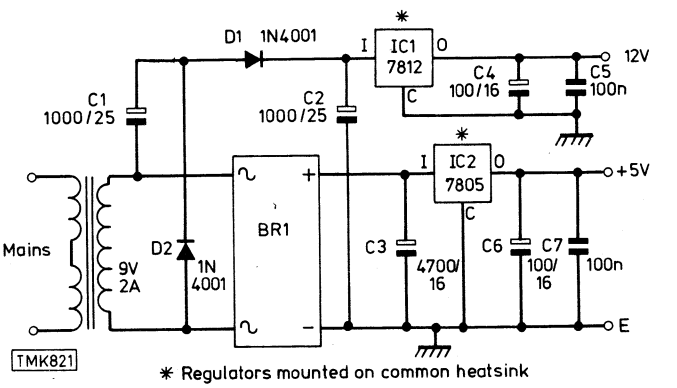

Fig. 8: Power supply circuit.

Another potential divider, in Q2's emitter circuit, reduces the signal to the level required to drive the UM1286 u.h.f. modulator. R11 sets the modulator's d.c. working point. This should be 2·2V: any significant departure from this voltage will cause sync crushing or even loss of sync. The value of R11 may need to be adjusted.

The modulator selected is a good-quality wideband type which also contains an intercarrier oscillator. If required, the frequency of this can be changed to 5·5MHz. An add-on audio oscillator will be described later. Constructors can if they wish use a CMOS divider circuit fed from the 7·8kHz output of IC5 to produce several frequencies, one of which can be fed directly to the modulator's audio input pin.

Power Supply

The power supply is straightforward, using a 7805 regulator to produce the 5V rail and a voltage doubler followed by a 7812 for the 12V rail. This arrangement is an economical design requiring only one mains transformer providing one secondary voltage, without excessive dissipation in the 5V regulator. Connect the transformer's primaries in series and the secondaries in parallel.