ARCHER®

TECHNICAL DATA

AN EXCLUSIVE RADIO SHACK SERVICE TO THE EXPERIMENTER

AY-3-1015D UNIVERSAL ASYNCHRONOUS RECEIVER/TRANSMITTER

DESCRIPTION

The Universal Asynchronous Receiver/Transmitter (UAR/T) is an LSI subsystem which accepts binary characters from either a terminal device or a computer and receives/transmits this character with appended control and error detecting bits. All characters contain a start bit, 5 to 8 data bits, one or two stop bits (1½ stop bit capability) and either odd/even parity or no parity. In order to make the UAR/T universal, the baud, bits per word, parity mode, and the number of stop bits are externally selectable. All inputs and outputs are directly compatible with MTOS/MTNS logic, and also with TTL/DTL/CMOS logic without the need for interfacing components. All strobed outputs are three-state logic.

FEATURES:

- DTL and TTL compatible — no interfacing circuits required — drives one TTL load
- Fully Double Buffered — eliminates need for system -synchronization, facilitates high-speed operation
- Full Duplex Operation — can handle multiple bauds (receiving-transmitting) simultaneously
- High Speed Operation
- Three-State Outputs — bus structure capability
- Low Power — minimum power requirements
- Input Protected — eliminates handling problems
- Single Supply Operation
- External reset of all registers except control bits register
- 0 to 30K baud
- Pull-up resistors to V_{CC} on all inputs

ELECTRICAL CHARACTERISTICS

Maximum Ratings*

V_{CC} (with respect to GND) . . . . . −0.3 to +16 V
Storage Temperature . . . . . −65°C to +150°C
Operating Temperature. . . . . 0°C to +70°C

*Exceeding these ratings could cause permanent damage. Functional operation of these devices at these conditions is not implied — operating ranges are specified below.

BLOCK DIAGRAM

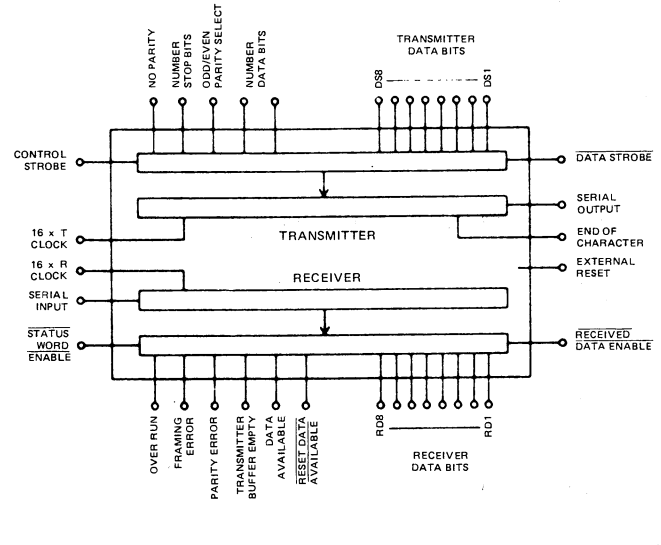
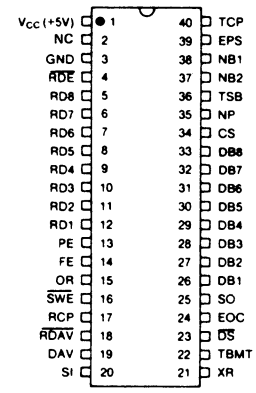


Figure 1

PIN CONFIGURATION

40 LEAD DUAL IN LINE

Top View



* Pin 2: No Connection.

PIN FUNCTIONS

PIN	NAME (SYMBOL)	FUNCTION
1	V_{CC} Power Supply (V_{CC})	+5V Supply
2		Not connected
3	Ground (V_{GI})	Ground
4	Received Data Enable (RDE)	A logic "0" on the receiver enable line places the received onto the output lines.
5-12	Received Data Bits (RD8-RD1)	These are the 8 data output lines. Received characters are right justified: the LSB always appears on RD1. These lines have tristate outputs, i.e., they have the normal TTL output characterisitics when RDE is "0" and a high impedance state when RDE is "1". Thus, the data output lines can be bus structure oriented.
13	Parity Error (PE)	This line goes to a logic "1" if the received character parity does not agree with the selected parity. Tri-state.
14	Framing Error (FE)	This line goes to a logic "1" if the received character has no valid stop bit. Tri-state.
15	Over-Run (OR)	This line goes to a logic "1" if the previously received character is not read (DAV line not reset) before the present character is transferred to the receiver holding register. Tri-state.
16	Status Word Enable (SWE)	A logic "0" on this line places the status word bits (PE, FE, OR, DAV, TBMT) onto the output lines. Tri-state.
17	Receiver Clock (RCP)	This line will contain a clock whose frequency is 16 times (16X) the desired receiver baud.
18	Reset Data Available (RDAV)	A logic "0" will reset the DAV line. The DAV F/F is only thing that is reset.
19	Data Available (DAV)	This line goes to a logic "1" when an entire character has been received and transferred to the receiver holding register. Tristate-Fig. 16.
20	Serial Input (SI)	This line accepts the serial bit input stream. A Marking (logic "1") to spacing (logic "0") transition is required for initiation of data reception. Fig. 15,16.
21	External Reset (XR)	Resets all registers except the control bits register. Sets SO, EOC and TBMT to a logic "1". Resets DAV and error flags to "0". Clears input data buffer. Must be tied to logic "0" when not in use.
22	Transmitter Buffer Empty (TBMT)	The transmitter buffer emtpy flag goes to a logic "1" when the data bits holding register may be loaded with another character. Tri-state. See Fig. 9, 11.
23	Data Strobe (DS)	A strobe on this line will enter the data bits into the data bits holding register. Initial data transmission is initiated by the rising edge of DS. Data must be stable during entire strobe.
24	End of Character (EOC)	This line goes to a logic "1" each time a full character is transmitted. It remains at this level until the start of transmission of the next character. See Fig. 8, 10.
25	Serial Output (SO)	This line will serially, by bit, provide the entire transmitted character. It will remain at a logic "1" when no data is being transmitted.
26-33	Data Bit Inputs (DB1-DB8)	There are up to 8 data bit input lines available.
34	Control Strobe (CS)	A logic "1" on this lead will enter the control bits (EPS, NB1, NB2, TSB, NP) into the control bits holding register. This line can be strobed or hard wired to a logic "1" level. See Fig. 19.
35	No Parity (NP)	A logic "1" on this lead will eliminate the parity bit from the transmitted and received character (no PE indication). The stop bit(s) will immediately follow the last data bit. It not used, this lead must be tied to a logic "0".
36	Number of Stop Bits (TSB)	This lead will select the number of stop bits, 1 or 2, to be appended immediately after the partiy bit. A logic "0" will insert 1 stop bit and a logic "1" will insert 2 stop bits. The combined selection of 2 stop bits and 5 bits/character will produce 1½ stop bits.
37-38	Number of Bits/Character (NB2, NB1)	These two leads will be internally decoded to select either 5, 6, 7 or 8 data bits/character. NB2 NB1 Bits/Character 0 0 5 0 1 6 1 0 7 1 1 8
39	Odd/Even Parity Select (EPS)	The logic level on this pin selects the type of parity which will be appended immediately after the data bits. It also determines the parity that will be checked by the receiver. A logic "0" will insert odd parity and a logic "1" will insert even parity.
40	Transmitter Clock (TCP)	This line will contain a clock whose frequency is 16 times (16X) the desired transmitter baud.

TRANSMITTER OPERATION

Initializing

Power is applied, External Reset is enabled and Clock pulse is applied having a frequency of 16 times the desired Baud. The above conditions will set TBMT, EOC, and SO to logic "1" (line is marking).

After initializing is completed, user may set control bits and data bits, with control bits selection normally occurring before data bits selection. However, one may set both DS and CS simultaneously if minimum pulse width specifications are followed. Once Data Strobe (DS) is pulsed, the TBMT signal will change from a logic "1", indicating that the Data Bits Holding Register is filled with a previous character and is unable to receive new data bits, and Transmitter **Shift Register** is transmitting previously loaded data. TBMT will return to logic "1".

When Transmitter Shift Register is empty, data bits in the Holding Register are immediately loaded into the Transmitter Shift Register for transmission. The shifting of information from the Holding Register to the Transmitter Shift Register will be followed by SO and EOC going to a logic "0"; and TBMT will also go to a logic "1", indicating that the shifting operation is completed and that the Data Bits Holding Register is ready to accept new data. If should be remembered that one full character time is now available for loading of the next character without loss in transmission speed due to double buffering (separate Data Bits Holding Register and Transmitter Shift Register).

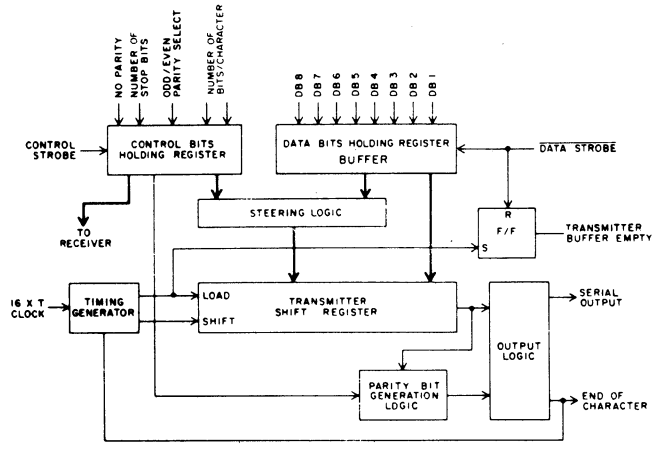


Fig. 2 TRANSMITTER BLOCK DIAGRAM

RECEIVER OPERATION

Initializing

Power is applied, External Reset is enabled, and Clock Pulse is applied having a frequency of 16 times the desired Baud. The previous conditions will set Data Available (DAV) to a logic "1".

After initializing is completed, user should note that one set of control bits will be used for both receiver and transmitter, making individual control bit setting unnecessary. Data reception starts when Serial Input signal changes from Marking (logic "1") to spacing (logic "0") which initiates start bit. The start bit is valid if, after transition from logic "1" to logic "0", the SI line continues to be at logic "0" (when center sampled) 8 clock pulses later. If, however, line is at a logic "1" when center sampling occurs, the start bit verification process will be reset. If the Serial Input line transitions from a logic "1" to a logic "0" (marking to spacing) when the 16x clock is in a logic "1" state, the bit time for center sampling will begin when the clock line transitions from a logic "1" to a logic "0" state. After verification of a genuine start bit, data bit reception, parity bit reception and stop bit(s), reception proceeds in an orderly manner.

While receiving parity and stop bit(s) the receiver will compare transmitted parity and stop bit(s) with control data bits (parity and number of stop bits) previously set and indicate an error by changing the parity error flip flop and/or the framing error flip flop to a logic "1". It should be noted that if the No Parity Mode is selected the PE (parity error) will be unconditionally set to a logic "0".

Once a full character is received, internal logic looks at the Data Available (DAV) signal to determine if data has been the read out. If the DAV signal is at a logic "1" the receiver will assume data has not been read out and the over run flip flop of the Status Word Holding Register will be set to a logic "1". If the DAV signal is at a logic "0" the receiver will assume that data has been read out. After DAV goes to a logic "1", the Receiver Shift Register is now ready to accept the next character and has one full character time to remove the received character.

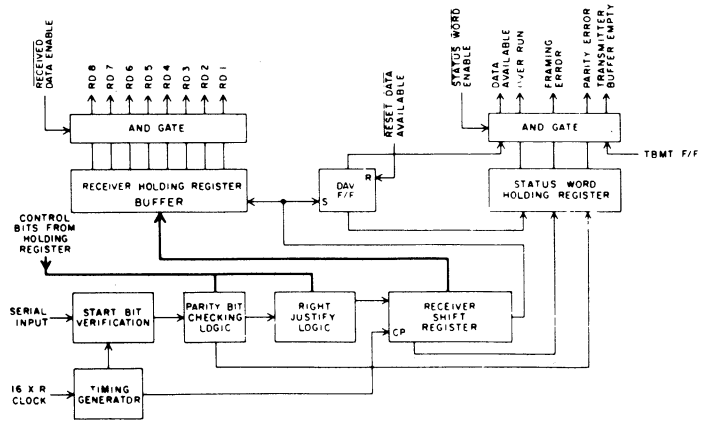


Fig. 3 RECEIVER BLOCK DIAGRAM

SPECIFICATIONS

Standard Conditions (unless otherwise noted)

V_{CC} = +4.75V to +5.25V

Operating Temperature (T) = 0°C to +70°C

Characteristics	Min	Typ**	Max	Units	Conditions
DC CHARACTERISTICS					
Input Logic Levels					
Logic 0	0	–	0.8	Volts	
Logic 1	2.4	–	V_{CC}+0.3	Volts	Has internal pull-up resistors to V_{CC}
Input Capacitance					
All inputs	–	–	20	pF	0 volts bias, f = 1MHz
Output Impedance					
Tri-State Outputs	1.0	–	–	MΩ	
Data Output Levels					
Logic 0	–	–	+0.4	Volts	I_{OL} = 1.6mA (sink)
Logic 1	2.4	–	–	Volts	I_{OH} = –40μA (source)–at V_{CC} = +5V
Output Capacitance	–	10	15	pF	
Short Ckt. Current	–	–	–	–	See Fig. 4.
Power Supply Current					
I_{CC} at V_{CC} = +5V	–	10	15	mA	
AC CHARACTERISTICS					T = 25°C, Output load capacitance 50 pF max.
Clock Frequency	DC	–	400	kHz	at V_{CC} = +4.75V/+14V
Baud	0	–	25	kbaud	at V_{CC} @ +4.75V/+14V
Pulse Width					
Clock Pulse	1.0	–	–	μS	See Fig. 14
Control Strobe	200		–	ns	See Fig. 19a
Data Strobe	200	–	–	ns	See. Fig. 18
External Reset	500	–	–	ns	See Fig. 17
Status Word Enable	500		–	ns	See Fig. 12
Reset Data Available	200	–	–	ns	See Fig. 13
Received Data Enable	500	–	–	ns	See Fig. 12
Set Up & Hold Time					
Input Data Bits	20	–	–	ns	See Fig. 18
Input Control Bits	20	–	–	ns	See. Fig. 19b
Output Propagation Delay					
TPD0	–	–	500	ns	See Fig. 12, 5
TPD1	–	–	500	ns	See Fig. 12, 5

**Typical values are at +25°C and nominal voltages.

TYPICAL CHARACTERISTIC CURVES

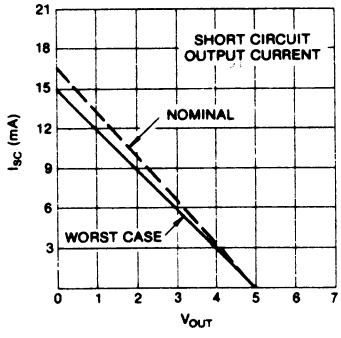


Fig. 4 SHORT CIRCUIT OUTPUT CURRENT (only 1 output may be shorted at a time)

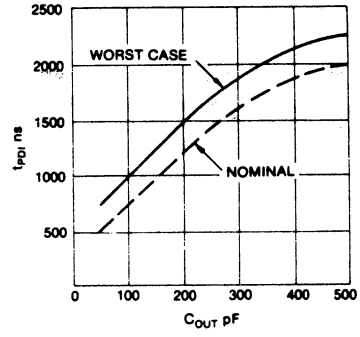


Fig. 5 RD1-RD8, PE, FE, OR, TBMT, DAV

APPLICATIONS

Note: The connection details of this device depend on the system you wish to interface with. Refer to standard reference books that are published by that particular system manufacturer.

COMPUTER INTERFACING

The strobing capability of the Universal Asynchronous Receiver/ Transmitter unit (UAR/T) makes it ideal for interfacing the unit into any of the popular computer systems. Since there are control and data transfer instructions provided by the CPU, two separate strobes are provided. They are the control strobe line and the data strobe line.

A typical computer interface will provide a unique device address to select a given device for an operation. The UAR/T is assigned one of the availlable addresses. When the UAR/T is selected, it will respond to one of the Computer I/O commands. These include Read, Write, Device Word, Control and Interrupt.

Read Command
This command will read the contents of the received data into the computer.

Write Command:
The write command will load the contents of the computer data out lines into the transmitter buffer.

Device Status Word
This command will read the status of the received data, that is the parity, framing, overrun, and end of transmit into the computer.

Control Command
This command will modify the UAR/T to respond to odd/even parity, number of bits/character, number of stop bits, or no parity.

Interrupt
The UAR/T provides two interrupt conditions which are Transmitter Buffer Empty and Data Available.

TERMINAL INTERFACING

If a terminal manufacturer would like to have his terminal compatible with as many other terminals and central processing units as possible, he can utilize the variable format of the UAR/T to make this possible. By means of strapping options or P.C. switches he could select the number of data bits (6-level or 7-level ASCII, for example), the type of parity, etc. In this way. each user could have a customized interface, yet the terminal manufacturer would have a standard interfacing card between his parallel-operating terminal and his asynchronous, serial operating modem.

Since the UAR/T is universally programmable through the five control pins and the control enable input, it can be used to interface with a wide variety of terminals, including Radio Shack's Models I, II and III.

TIMING DIAGRAMS

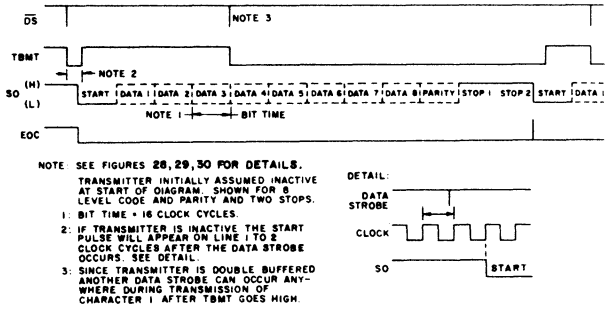


Fig. 6 UAR/T – TRANSMITTER TIMING

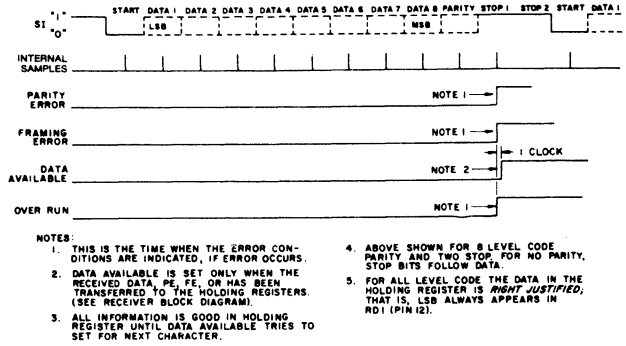


Fig. 7 UAR/T – RECEIVER TIMING

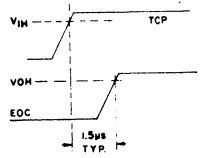


Fig. 8 EOC TURN-ON

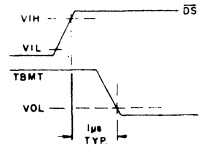


Fig. 9 TBMT TURN-OFF

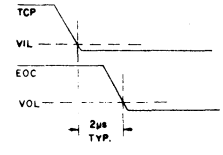


Fig. 10 EOC TURN-OFF

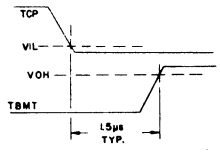


Fig. 11 TBMT TURN-ON

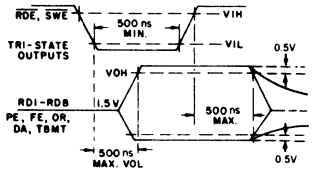


Fig. 12 RDE, SWE

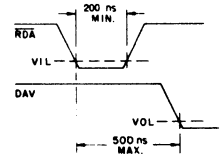


Fig. 13 RDAV

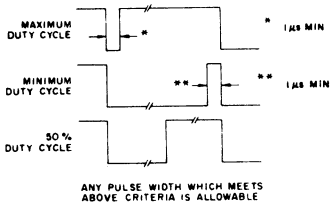


Fig. 14 ALLOWABLE TCP, RCP

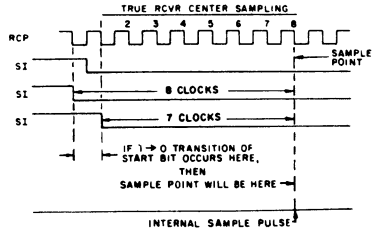


Fig. 15

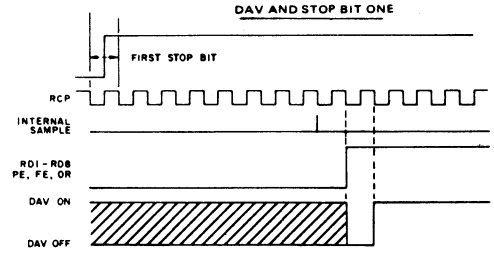


Fig. 16 RECEIVER DURING 1ST STOP BIT

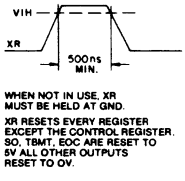


Fig. 17 XR PULSE

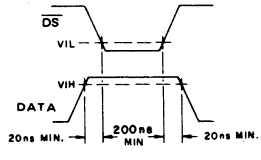


Fig. 18 DS

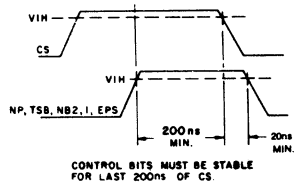


Fig. 19a CS

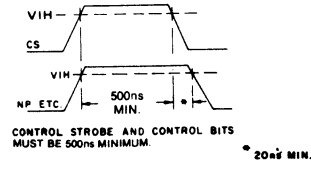


Fig. 19b

RADIO SHACK, A DIVISION OF TANDY CORPORATION

U.S.A.: FORT WORTH, TEXAS 76102
CANADA: BARRIE, ONTARIO L4M 4W5

TANDY CORPORATION

AUSTRALIA	BELGIUM	U. K.
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