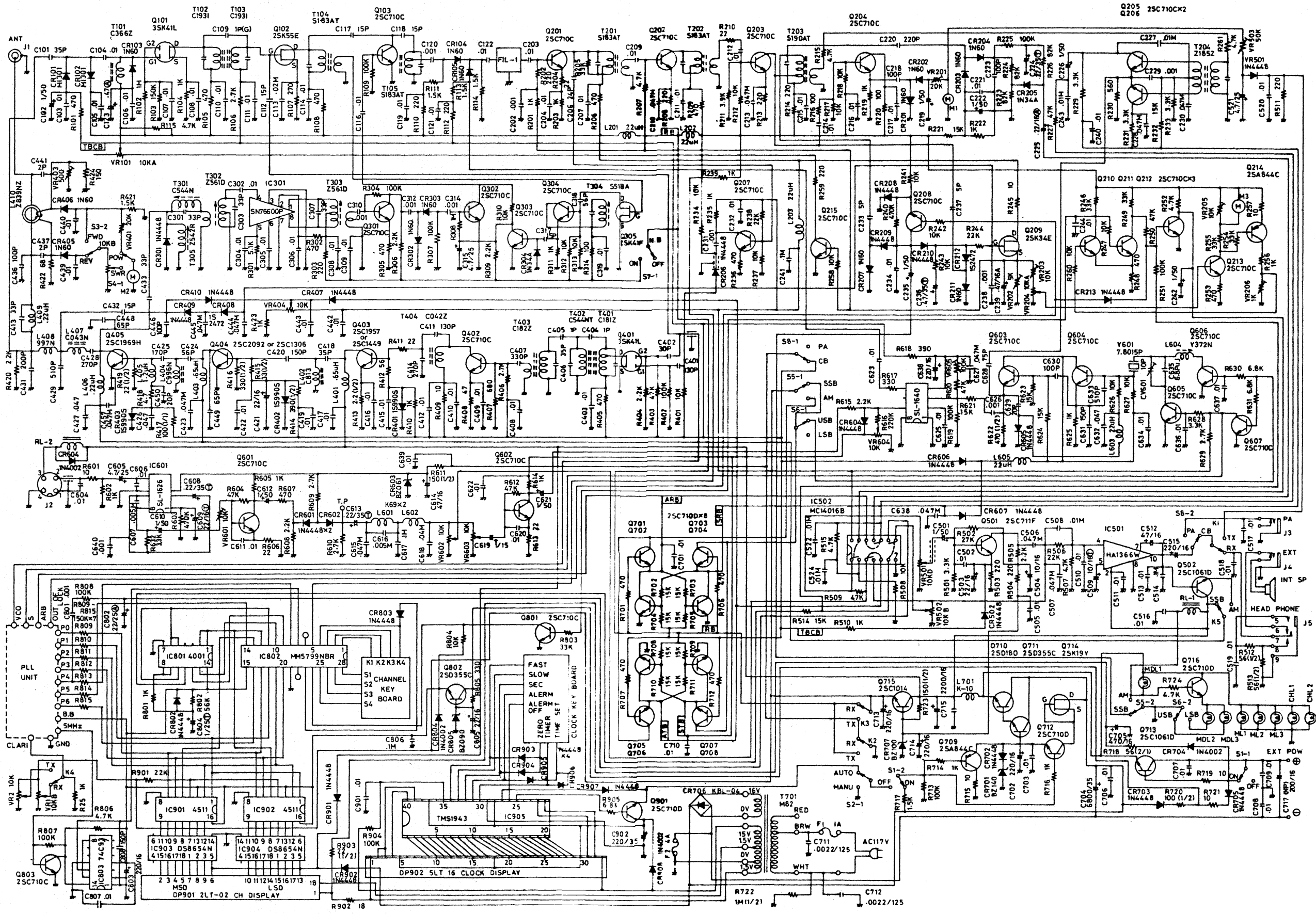


MAIN CIRCUIT DIAGRAM

Sidebander II



# PLL CIRCUIT DIAGRAM

sidebander VI

